

## Device and method for frequency synthesis with high spectral purity

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

5       The present invention relates to a device and method of synthesis with high spectral purity.

It relates especially to the variable division of a synthesizer with variable step size used to obtain high spectral purity and a constant frequency step size.

10       The schematic drawing of a phase-locked loop is given in figure 1. The loop comprises a voltage-controlled oscillator 1 (VCO) the phase of which has to be controlled in a feedback loop by a reference signal  $F_{ref}$ . For this purpose, the output of the VCO is divided by a frequency divider 2 and the divided VCO is compared to the reference frequency  $F_{ref}$  by means of a  
15       phase/frequency comparator 3. The error signal coming from the comparator is then filtered by the loop filter 4 which determines the stability of the feedback control loop. The VCO is controlled by a control voltage on which the filtered signal is superimposed. When the VCO is phase-controlled, the output frequency is equal to  $N \cdot F_{ref}$  where  $N$  is the rank of the  
20       divider. By making  $N$  vary from  $N_1$  to  $N_2$ , ( $N_2 > N_1$ ) in steps of 1, the VCO swings by steps of a size equal to  $F_{ref}$  in a frequency band corresponding to  $(N_2 - N_1) \cdot F_{ref}$ .

When it is sought to generate frequency steps smaller than  $F_{ref}$ , it is possible to reduce the value of  $F_{ref}$  but this has the consequence of  
25       augmenting the value of the division ranks and therefore of augmenting the phase noise of the synthesizer.

#### 2. Description of the Prior Art

The technique known as the fractional step synthesis technique resolves this problem. It is illustrated in figure 2 in a block diagram of a 160-  
30       320 MHz synthesizer.

It consists in obtaining a dynamic variation in the  $N$  division rank so as to generate, for example, a mean value  $N$  comprising a fractional part. For example, if one out of ten times, the division is performed by  $N+1$  instead of by  $N$ , the mean value  $N$  is equal to  $(N+1)/10$ . Since the rate of variation of  
35        $N$  is far greater than the band of the feedback control loop, the VCO is offset

by  $1/10$  of the frequency  $F_{ref}$ . This results in a phase variation  $2\pi/N$  at the phase/frequency comparator. This technique gives rise to parasitic lines at the output of the VCO. For a triple fractional step, which reduces the level of these parasitic lines, this variation goes to  $6\pi/N$ .

5           This variation must be kept below  $120^\circ$  especially if the phase comparator used is a diode-based mixer type of phase comparator associated with a frequency-searching device. This is to the use of minimum division ranks equal to about 10.

10           The synthesizer has a VCO covering the 160-320 MHz frequency band. The VCO divided by  $N$  is compared with a reference frequency of 20 MHz. A control signal  $N/N+1/N+2$  brings about variations, at a rate of 20 MHz, in the  $N$  division rank so as to generate steps at 100th of the value of the reference frequency (a double fractional step is used with modulo 2 equal to 4 and 25 so as to benefit from an additional attenuation on the first  
15 three fractional lines).

          However, this method has major drawbacks:

- 1) The VCO must cover a one-octave band, and this means that it is difficult to make,
- 2) The  $N$  divider too covers one octave, inducing a variation by 2 in the  
20 feedback loop gain, and this variation gets combined with the possible variations of slopes of the VCO and leads to increased complexity, because these variations have to be compensated for in order to maintain the switching time and the level of the parasitic lines throughout the frequency range,
- 23) The switching time of the synthesizer is limited because the control loop  
25 band must be below the value of the first fractional line (200 KHz in the example given) to be able to benefit from an additional attenuation of this line through the transfer function of the phase loop,
- 4) Since the minimum division rank is close to 10 and since the divider must  
30 cover one octave, the result is an increase of at least 26 dB in the phase noise as compared with the technological noise of the dividers.

          The invention relates to a method and a device that can be used especially to overcome the drawbacks of the prior art.

### SUMMARY OF THE INVENTION

The invention relates to a device to synthesize a frequency  $F1 \rightarrow F2$  with high spectral purity, comprising a synthesizer with a variable step  $F3 \rightarrow F4$ . It is characterized by the fact that it comprises at least one  
 5 variable rank divider  $N_b$  located after said synthesizer and a frequency control device delivering the division rank command of the variable rank divider, the command of the frequency of the variable-step synthesizer, the command of the synthesis step of the variable-step synthesizer.

The variable-step synthesizer is, for example, a fractional step  
 10 phase-locked loop synthesizer.

The variable-rank divider  $N_b$  takes the values  $N_1$  to  $N_p$ , these values following an arithmetic progression or a non-arithmetic progression.

The device may comprise a mixer receiving the output signal from the fractional step synthesizer and a mixing signal.

The invention also relates to a method to synthesize a frequency  $F1 \rightarrow F2$  with high spectral purity using a variable-step synthesizer  $F3 \rightarrow F4$ . It is characterized by the fact that it comprises at least one step in which the output signal of the variable-step synthesizer is transmitted to a multiple-rank divider  $N_p$  and by the fact that the division rank, the synthesis step of the  
 15 synthesizer and the frequency of the variable-step synthesizer are modified.  
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The invention offers especially the following advantages:

- it augments the performance of a fractional pitch synthesizer while being simple at the same time,
- it provides remarkably gain by reducing the relative band of the VCO,
- 25 • it improves spectral quality,
- it increases the switching speed of the synthesizer

### BRIEF DESCRIPTION OF THE DRAWINGS

Other features and advantages of the invention shall appear more clearly from the following description of a detailed example given by way of a  
 30 description that in no way restricts the scope of the invention, and from the appended drawings, of which:

- Figure 1 is a schematic drawing of the working of a fractional-step synthesizer ,
- Figure 2 is a block diagram of a prior art fractional-step synthesizer,

- Figure 3 is a block diagram of an exemplary device according to the invention,
- Figures 4 and 5 show alternative embodiments of the device of figure 3,
- Figure 6 shows a numerical example.

#### 5                    MORE DETAILED DESCRIPTION

In order to provide for a clearer understanding of the object of the present invention, the following example, which is given by way of an illustration that in no way restricts the scope of the invention, relates to a 160-320 MHz frequency synthesizer.

10                  The references given in figures 2, 3, 4 and 5 designate similar elements.

Figure 3 describes an exemplary device according to the invention, comprising, for example, a variable-step frequency synthesizer 10 that delivers a signal whose fundamental frequency ranges between a frequency F3 and a frequency F4. It comprises a variable-rank Nb divider 11  
15 that assumes the values N1 to Np (with  $N1 < N2 \dots < Np$ ), a control device 12 to control the output frequency and, as the case may be, a filter 13.

The control device 12 delivers the following commands:

- The command of the rank Nb of the variable-rank divider,
- 20    • The command of the frequency of the variable-step synthesizer which varies from F3 to F4,
- The command of the step of the variable-step frequency synthesis.

These three commands are, for example, implemented simultaneously in normal operation.

25                  The smallest value of the division rank Nb is chosen for example to be equal to N1. This value N1 determines the desired improvement of the spectral qualities of the variable-step synthesizer in terms of phase noise and parasitic lines. The smallest value N1 is chosen for example as a function of the template of the phase noise desired at total output and the template of  
30 the phase noise possible for the synthesizer located upstream from the divider. Indeed, the fact, of dividing by the division rank Nb, whose smallest value is N1, will improve the phase noise of the variable-step synthesizer by at least  $20\log(N1)$  dB.

The maximum frequency of the variable-step synthesizer is then given by  $F_4 = N_1 \cdot F_2$ ,  $F_2$  being the maximum output frequency of the device according to the invention.

If the sequence  $N_1 \dots N_p$  is chosen in arithmetic progression, the  
 5 minimum frequency of the variable-step synthesizer is given by  $N_2$ . For example,  $F_3$  is chosen to be substantially equal to or slightly smaller than  $(N_1/N_2) \cdot F_4$ .

If the values of the sequence  $N_1 \dots N_p$  do not follow an arithmetic progression, the different ratios obtained are compared by dividing two  
 10 consecutive elements of the sequence, that is  $N_1/N_2$ ,  $N_2/N_3$ , ...,  $(N_{p-1})/N_p$ . In other words,  $a$  being the smallest value of these ratios,  $F_3$  is chosen for example to be substantially equal to a smaller than  $aF_4$  or the closest value or a value slightly below it.

Thus, the fact of varying the rank  $N_b$  of the divider enables the  
 15 output band  $F_1 \rightarrow F_2$  to be covered continuously so that there is only a relatively limited band synthesizer ( $F_3 \rightarrow F_4$ ).

The different ratios  $N_1/N_2$ ,  $N_2/N_3$ , ...,  $(N_{p-1})/N_p$  are not equal as a general rule. Hence, the frequency ranges obtained from  $F_3 \rightarrow F_4$  in performing the divisions by  $N_1$ ,  $N_2$ , ...  $N_p$ , namely  $F_3/N_1 \rightarrow F_4/N_1$ ,  $F_3/N_2$   
 20  $\rightarrow F_4/N_2$ , ...,  $F_3/N_p \rightarrow F_4/N_p$  overlap each other partially; in other words, certain output frequencies may be obtained from two different division ranks  $N_b$ . In this case, to maximize the spectral performance of the device, the highest division rank  $N_b$  for example will be chosen.

To obtain the output frequency band  $F_1 \rightarrow F_2$  with a constant  
 25 frequency step  $\Delta F$ , the method modifies the division rank  $N_b$  and also the synthesis step of the variable-step synthesizer. In other words:

- when a division is made by  $N_1$ , the synthesis step of the variable-step synthesizer must be  $N_1 \Delta F$ ,
- when the division is made by  $N_2$ , the synthesis step of the variable-  
 30 step synthesizer must be  $N_2 \Delta F$ , and so on and so forth.

Thus, the range of frequencies  $F_1 \rightarrow F_2$  is covered with a constant frequency step  $\Delta F$ .

Figure 4 shows an exemplary embodiment of the device according to the invention.

The device comprises a fractional synthesizer having an architecture that is substantially identical to the one given in Figure 2 and shall not be described in detail, a variable divider 11 that divides by  $N_b$ , followed by optional filtering elements referenced 13. The variable-step synthesizer is formed, for example, by a fractional step phase-locked loop as described here above.

The fact of making this type of synthesizer work with variable step values is dictated by the need to obtain constant or substantially constant frequency steps values at output of the divider by  $N_b$ .

In a fractional step synthesizer, the frequency step is a fraction of the frequency  $F_{ref}$ . For example, to obtain a step equal to  $F_{ref}/5$ , the division rank  $N_a$  of the frequency synthesizer is made to evolve over a cycle of 5 periods of  $F_{ref}$ .

In the device according to the invention, the length of the cycle of evolution of  $N_a$  is variable and dependent on the value  $N_b$  (division value of the variable-rank divider). The reference frequency  $F_{ref}$  is chosen so that the desired fractional step values are obtained as follows:

- $F_{ref}$  is a function of sequence of the values  $N_1, N_2, \dots, N_p$  that may be assumed by  $N_b$ ,
- $F_{ref}/\Delta F$  must be a multiple of the LCM of  $N_1, N_2, \dots, N_p$ .

Thus, the numbers  $F_{ref}/N_1\Delta F, F_{ref}/N_2\Delta F, \dots, F_{ref}/N_p\Delta F$  are integers and define the different modulo values to be used for the fractional step in the respective cases where  $N_b$  is equal to  $N_1, N_2, \dots, N_p$ .

The term "modulo" is used because generally the fractional step is implemented by means of one or more accumulators for which the sum of the carry values commands the variations of the divider  $N_a$ .

For example, with a reference frequency of 20 MHz, 200 KHz steps are obtained with a modulo 100 value, and this value can be decomposed into two accumulators modulo 4 and modulo 25 so as to obtain a double fractional step.

The device according to the invention uses either a simple fractional step or a multiple fractional step. To this end, the device comprises for example one accumulator or several accumulators which shall be programmable modulo so as to achieve the variable step values necessary for the method according to the invention.

It is clear that any device allowing to realize a cyclical command of the division rank  $N_a$ , with the possibility of programming the length of the cycle, would be suitable.

Figure 5 shows an alternative embodiment of the device of figure 4.

5 This variant consists in including a frequency transposition step in the fractional phase loop between the VCO and the divider  $N_a$ . The transposition frequency is a multiple of  $\Delta F$  multiplied by the LCM of the values of the division rank  $N_b$ . It is obtained by the addition, to the device, of the mixer 14 receiving the output signal from the VCO as well as the  
10 transposition frequency. The transposed signal is then transmitted to the divider 2.

Figure 6 illustrates a numerical example in which a device according to the invention is obtained with a 160-320 MHz frequency synthesizer .

In this example,  $N_b = 9, 10, 12, 15$ , and the band of the VCO varies  
15 from 2304 to 2880 MHz to obtain the 160-320 MHz band in continuity.

To obtain a constant step size of 200 KHz at output, the fractional synthesizer must be capable of generating steps of 1.8 MHz, 2 MHz, 2.4 MHz, and 3 MHz.

The LCM of  $N_b$  is equal to 180.  $F_{ref}$  should therefore be a multiple of  
20 36 MHz.

A value of 144 MHz is chosen and the different modulo values to be obtained, namely 80, 72, 60 and 48, are deduced therefrom.

These modulo values may be decomposed into 2 for a double fractional step embodiment:  $80 = 5 \times 16$ ,  $72 = 8 \times 9$ ,  $60 = 5 \times 12$ ,  $48 = 3 \times 16$ .

25 The following table 1 summarizes the performance obtained with a prior art synthesizer.

CHARACTERISTIC	PERFORMANCE
Relative band of the VCO ( $B/F_o$ )	67%
Increase of the noise relative to $F_{ref}$ + comparator noise	$+ 20 \log (N_{max}) = 26 \text{ dB}$
Gain on the phase noise of the VCO	0 dB
Frequency deviation of the parasitic line located at the boundary of the loop band	200 KHz
Attenuation of the first parasitic line located at the boundary of the loop band	58 dB @ 200 KHz

Table 2 gives the results obtained with the new method and gives the gain on this example relative to the prior art.

CHARACTERISTIC	PERFORMANCE	GAIN OVER THE PRIOR ART
Relative band of the VCO	22,2%	Relative band divided by 3
Increase in noise	$+ 20 \log (N_{\max}/N_{\min}) = 6,94 \text{ dB}$	Gain of 19 dB on the phase noise
Gain on the VCO noise	$20\log(N_{\min})$	Gain of 19 dB (limited by the lower-limit phase noise of $N_b$ )
Frequency difference of the closest parasitic line	1,8 MHz => possibility of a wide loop band	Gain by a ratio 9 on the switching speed
Attenuation of the first line located at the boundary of the loop	81 dB @ 1,8 MHz	Most efficient rejection of the fractional lines + 23 dB on the first

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It can thus be seen that the proposed method is simple to implement and that it provides remarkable gain in terms of:

- diminishing the relative band of the VCO,
- improving the spectral quality
- 10 • increasing the switching speed of the synthesizer

Without departing from the framework of the invention, any device that gives a variable step can be used. Such a device could be, for example, a fractional step synthesizer etc. or any other device known to those skilled in the art.